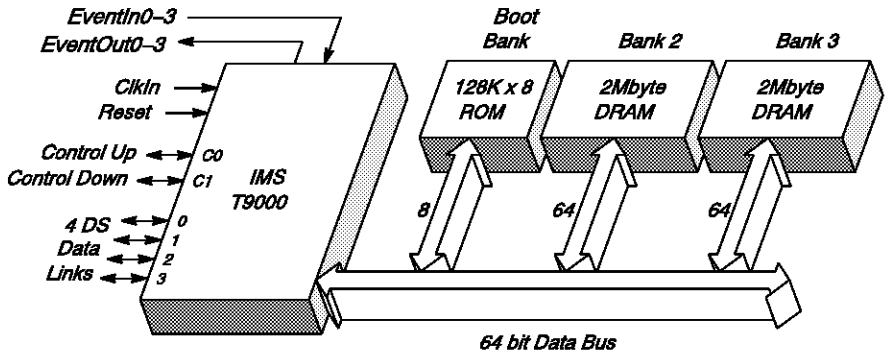
SGS-THOMSON MICROELECTRONICS

IMS B926

4 MBYTE HTRAM



FEATURES

- Easy to use system supercomponent module
- Integral low profile heatsink
- IMS T9000 processor provides up to 120MIPS and 15MFLOPS (30MHz processor).
- 4Mbytes fast, cacheable DRAM
- On-board configuration ROM
- Size 2 HTRAM, compatible with HTRAM motherboards
- Easily interfaced with other HTRAMs or IMS T9000s to build powerful multiprocessor systems
- 4 DS data links each provide 100Mbits/s communication with other IMS T9000s or HTRAMs
- Compilers and development tools available for ANSI C, C++, and occam 2.

DESCRIPTION

The IMS B926 is a second generation transputer module (HTRAM), which integrates the high performance IMS T9000 microprocessor with 4Mbytes of fast DRAM. The memory is organised as two 64-bit wide banks, both of which are cacheable. The memory system performs automatic page mode accesses whenever possible to provide maximum memory bandwidth.

An on-board ROM provides for local configuration of the IMS T9000 programmable memory interface and cache, and also contains identification data.

The IMS B926 is part of a family of HTRAMs and HTRAM motherboards and is an ideal building block for multiprocessor systems based on the IMS T9000.

The IMS B926 complies fully with the HTRAM Specification.

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1.1 Introduction

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1.2 The IMS B926 specification

The IMS B926 is one of a family of INMOS HTRAM products and complies fully with the published standard specification for HTRAM devices [1]. In terms of this specification it is a size 2 module offering a high performance computational supercomponent consisting of an IMS T9000 processor and 4Mbytes of DRAM in a robust and easy to use form. A dimensional diagram is given in figure 1.1.

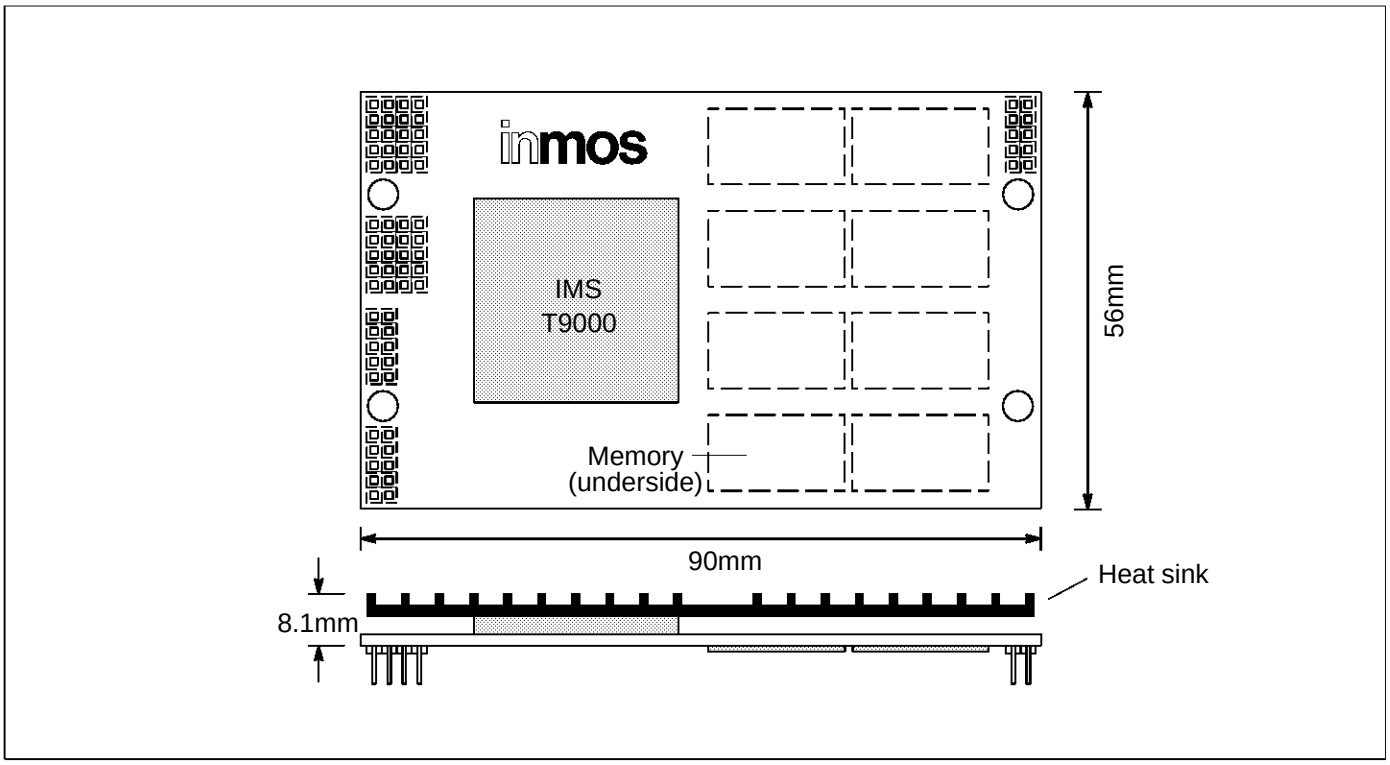

Figure 1.1 IMS B926 dimensions

Note: For full information on component height refer to [1].

1.2.1 Memory configuration

The memory organisation of the IMS B926 optimises performance of the IMS T9000 and its cache subsystem. The memory appears as two contiguous 2Mbyte banks on a 64bit wide data bus. The memory system performs automatic page mode accesses whenever possible to optimise memory bandwidth. The memory map of the IMS B926 is shown in figure 1.2.

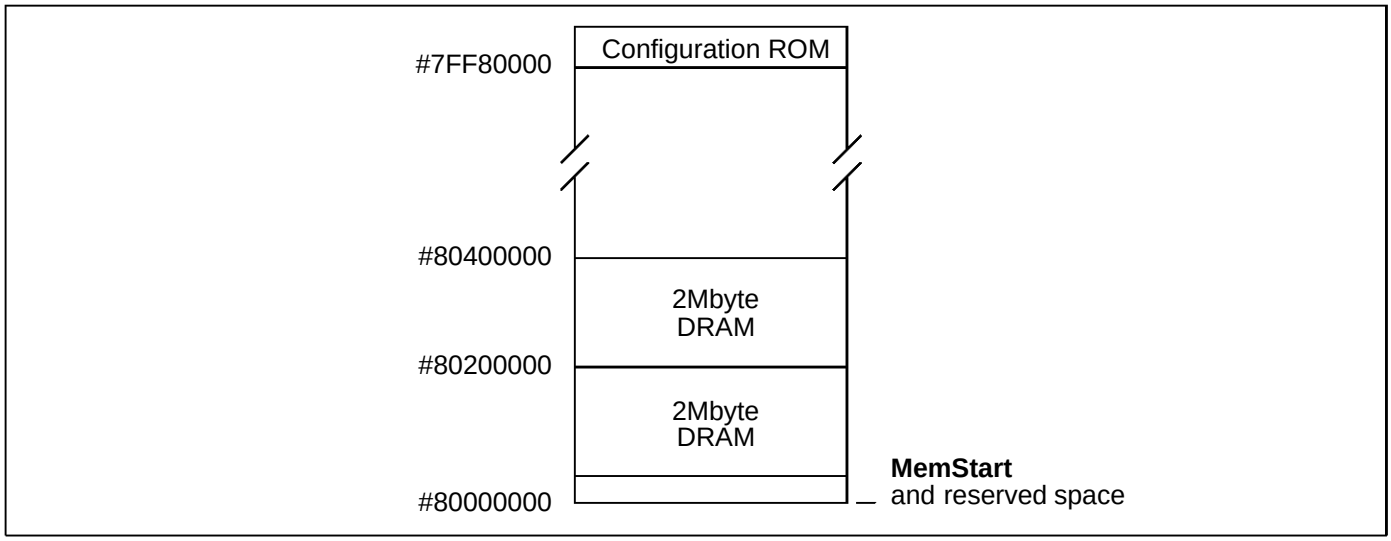

Figure 1.2 IMS B926 memory map

1.3 Interface Signals

The interface signals are as follows. Full electrical details can be found in [1] and [2].

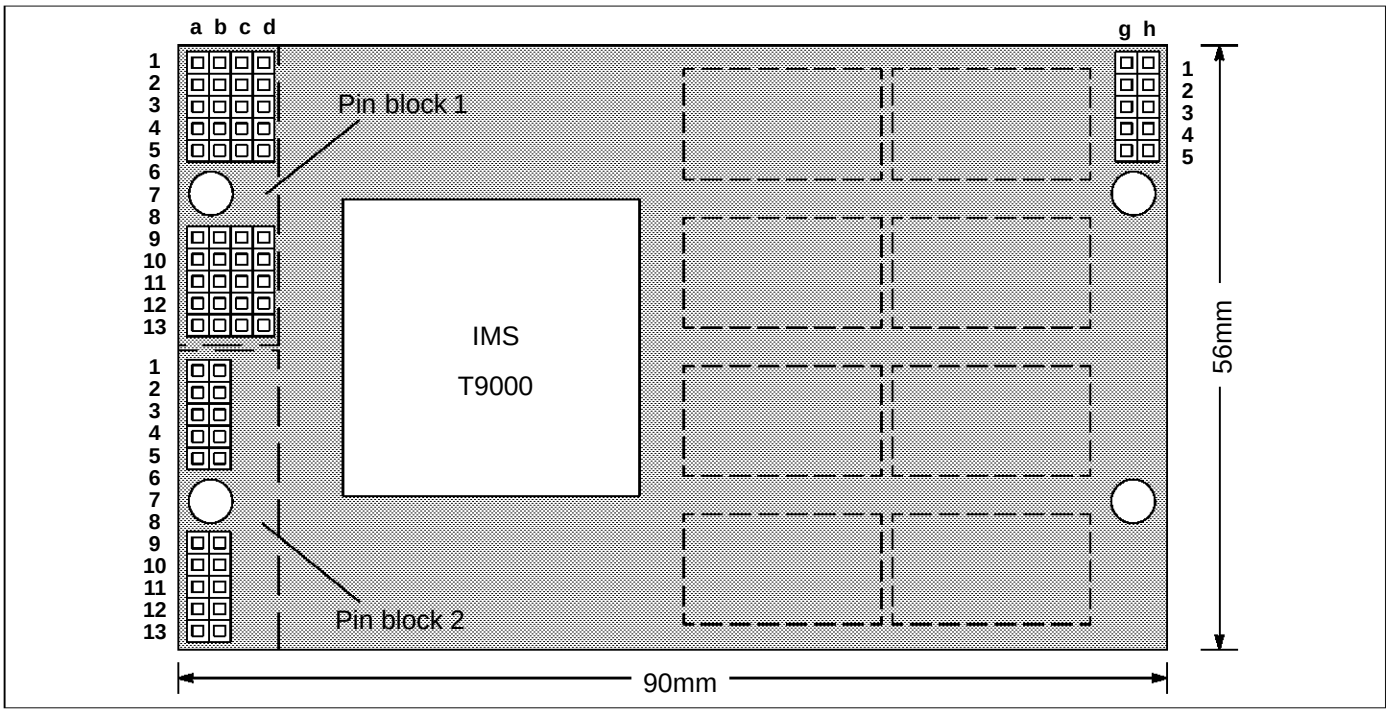

Figure 1.3 Size 2 HTRAM pinout configuration

Pin	Row a	Row b	Row c	Row d	Row g	Row h
1	ClkIn	N/C	TDI	notTRST	EventIn0	EventOut0
2	L0SIn	GND	V5V0	L2SOut	EventIn1	EventOut1
3	L0DIn	N/C	CUpSIn	L2DOut	EventIn2	EventOut2
4	L0DOut	V3V3	GND	L2DIn	EventIn3	EventOut3
5	L0SOut	N/C	CUpDIn	L2SIn	–	–
9	L1SIn	N/C	CUpDOut	L3SOut		
10	L1DIn	V5V0	GND	L3DOut		
11	L1DOut	N/C	CUpSOut	L3DIn		
12	L1SOut	GND	V3V3	L3SIn		
13	Reset	TMS	TCK	V5V0		
1	N/C	TDO				
2	N/C	GND				
3	N/C	CDnSOut				
4	N/C	V3V3				
5	N/C	CDnDOut				
9	N/C	CDnDIn				
10	N/C	V5V0				
11	N/C	CDnSIn				
12	N/C	GND				
13	N/C	N/C				

Table 1.1 IMS B926 Pinout reference

Signal name	Description
ClkIn	5MHz clock: the IMS T9000 generates its own high speed clocks.
Reset	IMS T9000 Reset: refer to [2] for a complete description of the IMS T9000 reset behavior.
LxDIn, LxSIn, LxDOut, LxSOut	The IMS B926 has four data links, connected directly to the corresponding IMS T9000 data links. Each data link consists of four signals, for example link 0 consists of **L0DIn, L0SIn, L0DOut, L0SOut**, and is data link 0 of the IMS T9000. Unused links may be left unconnected. Link connections should be designed as 100Ω transmission lines: no termination is required at either end, as the drivers and receivers are designed to work with unterminated lines.
CUpDIn, CUpSIn, CUpDOut, CUpSOut	The Control Up link is **Clink0** of the IMS T9000. It is used at system start time to initialize the IMS T9000, and must be connected to a suitable source of control messages: for example the Control Down link of another HTRAM in a daisy chain control architecture.
CDnDIn, CDnSIn, CDnDOut, CDnSOut	The Control Down link is **Clink1** of the IMS T9000. The Control Down link may be used to drive the Control Up link of another HTRAM or **Clink0** of an IMS T9000, in a daisy chain control architecture. Control Down may be left unconnected if daisy chain control is not being used, or for the last HTRAM in a control chain.
TMS, TCK, TDI, TDO, notTRST	These form an IEEE1149.1 test access port (TAP). The TAP on the IMS B926 is not implemented: **TMS and TCK** must be tied high, **notTRST** must be tied low, **TDI** should be tied high or connected to the TDO pin of another HTRAM. **TDO** may be left unconnected or connected to the TDI pin of another HTRAM. Pull-ups/pull-downs of up to 10kΩ may be used.
V5V0	The IMS B926 requires a 5.0V power supply to be connected to the **V5V0** and **GND** pins: all of these pins should be connected.
V3V3	The IMS B926 does not require a 3.3V power supply to be connected to the **V3V0** pins: these pins are not electrically connected on the IMS B926.
GND	Signal reference and power supply return pins.
EventIn0–3	Event (Interrupt) Inputs of the IMS T9000. Unused EventIn pins may be left unconnected as there is a pull-down resistor on each input.
EventOut0–3	Event Outputs of the IMS T9000. These signals function as Interrupt acknowledge signals in response to the corresponding EventIn, or can be used as outputs depending on the programming of the IMS T9000.

Table 1.2 Signal descriptions

1.4 Configuration and ID ROM

All HTRAMs have an ID ROM which can be used to identify the HTRAM in an assembled system. The identification data format is defined in [1]. The identification data for the IMS B926 is shown in table 1.3. For details on how to access this data, please refer to [1].

Data Item	Value
IdDataHeader	#44495448
IdDataVersion	#00000001
VendorString	SGS-THOMSON Microelectronics Limited
HTRAMtype	IMS B926-XXV
Serial Number	Unique per device
NumObjects	Subject to change
Objects	IMS_htram_NDL IMS_htram_MEM IMS_selftest_CODE
Note: HTRAM type include: XX – speed variant V – manufacturing variant	

Table 1.3 ID ROM data

This ROM also contains a configuration program to initialize the PMI bank address, PMI strobe timing, and Cache subsystems of the IMS T9000. The configuration program can be caused to execute by issuing a Reboot command to the **ControlUp** link of the IMS B926 during system initialization. The configuration program terminates by sending an Error message to the control process. The initialization of other IMS T9000 subsystems is system dependent, and should be made by a controlling process over the control up link.

1.5 Software Support

Toolsets are available for developing applications for single and multiprocessor systems in a variety of languages, including ANSI C, C++, and occam 2. The Toolsets contain a comprehensive collection of software development tools, such as:

- Optimizing compilers
- Tools for creating and loading multi-processor programs
- Extensive libraries
- Mixed language programming support
- Powerful debugging and profiling tools for single and multiprocessor systems.

The Toolsets are available for a variety of host systems, including Sun-4 and IBM PC. Please refer to [3] and [4] for full details on the T9000 Toolset products, and development platform hardware requirements.

1.6 Summary of features

Feature		Unit	Note
HTRAM type	IMS B926		
Processor type and speed	IMS T9000-*XX*		1
Memory size	4	Mbyte	
Cache size	16	Kbyte	
Memory organisation	Two 64-bit banks		
Memory cycle time	2–5	Cycles	2
Cache Configuration	from local ROM		
PMI Configuration	from local ROM		
StartFromROM	no		
Test Access Port	inactive		
Application specific pins	EventIn/EventOut		
HTRAM size	2 (56mm 90mm)		
Height class	B		
Weight	38	g	

Notes:

1 Note that *XX* denotes processor speed variation

2 Dependent upon the type of memory access being performed

Table 1.4 Specification

1.7 Electrical ratings and operating Ranges

Functionality is not guaranteed outside th Operating Ranges. Operation beyond the Operating Ranges is not recommended and may affect device reliability.

Parameter	Min.	Typ.	Max.	Unit
Operating temperature	0		50	°C
Airflow	TBD	2		m/s
V5V0	4.75	5.0	5.25	V
Input Voltage (any input)	0		V5V0	V
Power consumption (V5V0)		5	TBD	W
Power consumption (V3V3)			0	W

Table 1.5 Operating Ranges

1.7.1 Absolute Maximum Ratings

This is a stress rating only and functional operation of the HTRAM at these, or any other conditions beyond the operating range is not implied. Stresses beyond the Absolute Maximum Ratings may cause permanent damage.

Parameter	Min.	Max.	Unit
Storage temperature	0	70	°C
V5V0 relative to GND	0	7.0	V
Voltage on any pin relative to GND	–0.5	V5V0+0.5	V

Table 1.6 Absolute Maximum Ratings

1.8 Ordering Information

Please contact your local sales office or distribution representative for ordering information.

Description	Order Number
4Mbyte HTRAM	IMS B926–*XX**

Table 1.7 Ordering information

*Note: *XX* refers to processor speed variants. Consult your sales representative for details.

1.9 Field Support

INMOS products are supported worldwide through SGS-THOMSON Sales Offices and authorized distributors.

1.10 References

1 *HTRAM specification*, INMOS Ltd 1994

2 *T9000 Transputer Hardware Reference Manual,* INMOS Ltd 1993

3 *IMS Dx394 T9000 ANSI C Toolset datasheet*, INMOS Ltd 1994

4 *IMS Dx395 T9000 occam 2 Toolset datasheet*, INMOS Ltd 1994

5 *T9000 Brochure,* INMOS Ltd 1993

6 *The Transputer Development and i***q** *systems Databook* INMOS Ltd (72-TRN-219-01)